CLAIMS

What is claimed is:

1. A semiconductor integrated circuit comprising:

a K-bit (K is an integer not less than 2) data bus to which data is input;

a selection circuit selecting data input through one of an N number of lines on a high bit side and an N number of lines on a low bit side of the data bus in accordance with a set signal when N-bit data (N is an integer smaller than K) is input to the data bus; and

a random access memory (RAM) storing data selected by the selection circuit.

2. The semiconductor integrated circuit according to Claim 1, wherein the selection circuit further comprises:

a first selection circuit selecting a plurality of bits from the input N-bit data in accordance with a signal which is set in response to the number of N bits of the input data; and

a second selection circuit selecting an N number of bits from the plurality of bits output from the first selection circuit and supplying the bits to the RAM in accordance with a signal which is set so as to correspond to any desired one of the high bit side lines and the low bit side lines of the data bus.

3. The semiconductor integrated circuit according to Claim 1, wherein the selection circuit further comprises:

a first selection circuit selecting data input through one of a plurality of lines on the high bit side and a plurality of lines on the low bit side of the data bus in accordance with a signal which is set so as to correspond to any desired one of the high bit side lines and the low bit side lines of the data bus; and

a second selection circuit selecting an N number of bits from data output from the first selection circuit and supplying the bits to the RAM according to a signal which is set in response to the number of N bits of the input data.